STRUCTURE FOR REDUCED GATE CAPACITANCE IN A JFET

FIELD OF THE INVENTION

The present claimed invention relates to the field of junction field effect transistors (JFETs). More particularly, the present claimed invention relates to a reduction in the input capacitance of JFETs.

BACKGROUND ART

Junction field effect transistors (JFETs) are majority carrier devices that conduct current through a channel that is controlled by the application of a voltage to a p-n junction. JFETs may be constructed as p-channel or n-channel and may be operated as enhancement mode devices or depletion mode devices.

The most common JFET type is the depletion mode type. The depletion mode device is a normally "on" device that is turned off by reverse biasing the p-n junction so that pinch-off occurs in the conduction channel. P-channel depletion mode devices are turned off by the application of a positive voltage between the gate and source (positive V_{gs}), whereas n-channel depletion mode devices are turned off by the application of a negative voltage between the gate and source (negative V_{gs}). Since the junction of a depletion mode JFET is reverse biased in normal operation, the input voltage can be relatively high. Devices are available with input voltages with a magnitude greater than 100 volts.

Enhancement mode, or normally "off" JFETs are characterized by a channel that is sufficiently narrow such that a depletion region at zero applied voltage extends across the entire width of the channel. Application of a forward bias reduces the width of the depletion region in the channel, thereby creating a conduction path in the channel. P-channel enhancement mode JFETs are turned on by the application of a negative V_{gs}, and n-channel enhancement mode JFETs are turned on by the application of a positive V_{gs}. The input voltage of an enhancement mode JFET is limited by the forward breakdown voltage of the p-n junction.

Historically, JFETs have been used for analog switches, radio frequency devices, current regulators and high input impedance amplifiers, while logic circuits such as microprocessors have been the domain of metal oxide semiconductor field effect transistors (MOSFETs) as exemplified by complementary metal oxide semiconductor (CMOS) technology.

Traditionally, JFETs have been used as discrete devices or as input stages on integrated circuits such as operational amplifiers. However, as circuit complexity, operating frequency, and power management requirements have increased for CMOS devices such as microprocessors, it has become desirable to integrate power management and conditioning functions on the same die with the logic. JFETs are candidates for performing these functions

A transistor structure that is integrated on a logic circuit for the purpose of power management and conditioning will be faced with a requirement for high frequency operation and low power consumption. For field effect transistors (FETs), parasitic capacitances between the gate and source (C_{gs}) and gate and drain (C_{gd}) are significant factors affecting performance in this regard. In general, a low gate capacitance is desirable for transistors used in both analog and digital circuits. A low capacitance provides faster switching, higher frequency response and lower current and power requirements.

Although the characteristics of JFETs qualify them as candidates for integration with high speed logic circuits having sophisticated power management requirements, the conventional JFET device structures and processes are not optimized for such integration. The structures and processes that have heretofore been used to produce discrete devices or analog integrated circuits were not designed for integration with CMOS structures and processes.

Thus, a need exists for a JFET with minimal parasitic capacitances C_{gs} and C_{gd}. There is also a need for method for producing an optimal JFET structure that is compatible with the process flow used for logic integrated circuits.

SUMMARY OF INVENTION

Accordingly, embodiments of the present invention include a JFET structure that has reduced C_{gs} and C_{gd} and provides improved performance at high frequencies and greater power efficiency. Another aspect of the invention is a fabrication method that is readily integrated with a conventional process flow for logic integrated circuits. These and other objects and advantages of the present invention and others not specifically recited above will be described in more detail herein.

In an embodiment of the present invention, a gate definition spacer is formed on the wall of an etched trench to establish the lateral extent of an implanted gate region for a JFET. After implant, the gate is annealed. In addition to controlling the final junction geometry and thereby reducing the junction capacitance by establishing the lateral extent of the implanted gate region, the gate definition spacer also limits the available diffusion paths for the implanted dopant species during anneal. The net result is that the interfacial area between the gate and source and gate and drain are reduced, thereby reducing the associated parasitic capacitances C_{gs} and C_{gd}.

In another embodiment of the present invention, a gate region is formed by implanting and annealing. After annealing, a portion of the gate structure that is not directly adjacent to the channel is removed, thereby decreasing the parasitic capacitance C_{gd} between the gate and drain.

These and other objects and advantages of the present invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiments which are illustrated in the various drawing figures.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1**A shows a general schematic for an n-channel depletion mode junction field effect transistor (JFET).

FIG. **1**B shows a general schematic for an n-channel enhancement mode junction field effect transistor (JFET).

FIG. **2**A shows a JFET substrate prior to gate implant.

FIG. **2**B shows a JFET substrate after gate implant and prior to anneal.

FIG. **2**C shows a JFET substrate after anneal.

FIG. **3**A shows a JFET substrate with a gate definition spacer oxide prior to gate implant in accordance with an embodiment of the present claimed invention.

FIG. **3**B shows JFET substrate with a gate definition spacer oxide after gate implant and prior to anneal in accordance with an embodiment of the present claimed invention.

FIG. **3**C shows a JFET substrate after anneal in accordance with an embodiment of the present claimed invention.